REMARKS

Reconsideration of this application, in view of the foregoing amendments and the following remarks, is respectfully requested.

Drawings

The drawings are objected to because reference characters "10" and "14" have both been used to designate the entire system.

Applicant has submitted herewith a replacement sheet correcting the identified informality.

Specification

The Examiner has stated that "[t]he attempt to incorporate subject matter into this application by reference to "The CORDIC Trigonometric Computing Technique" by Jack Volder on page 10, lines 5-7 is improper because no copy was submitted as part of the information disclosure statement." Applicant respectfully point to the Examiner that the subject matter of the identified reference is not incorporated by reference in the identified sections of the specification. The subject matter was identified as the state of the art for background purpose for one skilled in the art. Therefore, the specification adequately describes the subject matter of the invention.

As to the reference number of the channel estimator, Applicant has amended the specification to remove the informality.

Claim Rejections - 35 USC §112

Claim 28 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant respectfully traverses this rejection.

The Examiner has stated that the specification does not support the subject matter recited in claim 28. Applicants respectfully points to the Examiner that on specification on page 17 with

reference to figure 7, step 708, clearly states that the phase offset is iteratively calculated without performing a trigonometric calculation. Therefore, claim 28 is fully supported by the specification. Further, claim 26 has been amended to include steps for calculating the offset phasor.

Claim Rejections - 35 USC §103

Claims 1-21, 26, 27 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagayasu et al., US Patent No. 6,347,126. Applicant respectfully traverses these rejections.

There are three basic criteria to establish a *prima facie* case of obviousness under 35 U.S.C. §103(a). First, there must be some suggestion or motivation in the cited references to modify or combine their teachings; second, there must be reasonable expectation of success; and third, the prior art references must teach or suggest all the claim limitations. *See* M.P.E.P §2142. As to claim 1, Nagayasu et al. neither teaches or suggests all the claim limitations nor provides motivation to modify its disclosure as the Examiner has asserted.

Regarding claim 1, the Examiner has stated that Nagayasu discloses "a channel estimator component (See figure 1) operative to process a data signal to form **a current channel impulse response** (See figure 1, blocks 12 and 14) and **a channel estimate**;" (emphasis added).. Applicants respectfully disagree. Blocks 12 and 14 are channel impulse response (CIR) estimators and they only estimate CIR at different positions in a received burst (*see* col. 8, lines 30-43). In contrast, claim 1 recites a channel estimator component operative to process a data signal to form a current channel impulse response **and** a channel estimate. Blocks 12 and 14 of Nagayasu et al. do not provide a channel estimate as recited in claim 1.

Further, the Examiner has stated that Nagayasu et al. describe "an offset phasor determiner (See figure 1, block 15 and column 8, lines 45-50) that determines an offset phasor as a function of the **current channel impulse response** and **a previous channel impulse response**" (emphasis added). Applicant respectfully disagree and point to the Examiner that Nagayasu et el. describe block 15 as a phase deviation circuit that estimates values at two different positions determined by channel impulse response estimating circuits 12 and 14. According to Nagayasu et al., these circuits estimate channel impulse response at two different

positions within the same burst in a corrected received signal r'_n (*see* col. 8, lines 30-34 for unit 12; and col. 8, lines 38-43 for unit 14). In contrast, claim 1 recites an offset phasor determiner that determines an offset phasor as a function of the current channel impulse response and a previous channel impulse response. Thus, Nagayasu et al. does not teach an offset phasor as a function of the current channel impulse response and a previous channel impulse response as recited in claim 1. Accordingly, claim 1 is patentably distinguishable from Nagayasu et al.

Further, the Examiner has stated that

> "Nagayasu fails to disclose a phase offset corrector that provides a phase corrected channel impulse response to the channel estimator, such that the channel estimator determines a corrected channel estimate. However, he discloses a **frequency offset corrector** that provides a **phase corrected** channel impulse response to the **channel estimator**, such that the channel estimator determines a corrected channel estimate. It would be obvious to one of ordinary skill in the art to use a phase corrector in place of a frequency corrector. One could be motivated to do this since phase and frequency have a linear relationship." (Emphasis added).

Applicants respectfully point to the Examiner that first, Nagayasu et al. is directed to and describes a receiver with a frequency offset correcting function (*see* col. 3, line 62 – col. 4, line 3). The frequency offset correcting circuit 11 depends on a frequency offset estimated value $\Delta\acute{\omega}_m$ received from the averaging circuit 16. If a phase corrector is used in place of the frequency corrector as the Examiner has asserted, then the entire circuit of Nagayasu et el. will have to be changed because a phase corrector will need different offset from the averagor because an ordinary person skilled in the art will not just replace a frequency corrector with phase corrector.

Further, the functions of the CIR estimating circuits have to be modified, furthermore, the equalizer needs to be adjusted to respond to the phase corrected input rather than frequency corrected signal. Similarly, rest of the functions of the circuit will have to be modified to convert the frequency offset correcting function to a phase offset correcting function as the Examiner has asserted. This will basically change the entire circuit of Nagayasu et al. "The proposed modification cannot render the prior art unsatisfactory for its intended purpose." *See* MPEP §2143.01. The Examiner's suggestion is hindsight reconstruction of Nagayasu et al.'s circuit, which renders Nagayasu et al. inoperative for its intended purpose of improving the capabilities

of transmission using frequency offset correcting circuit. Accordingly, claim 1 is not obvious in view of Nagayasu et al. and thus, clearly patentably distinguishable from Nagayasu et al.

Claims 2-7 depend from claim 1 and are patentably distinguishable from Nagayasu et al for at least the same reasons as claim 1.

Further regarding claim 2, the Examiner has stated that "one can appreciate that in order for the system to calculate the offset, it would have to "store" the previous channel impulse response." Applicants respectfully point to the Examiner that claim 2 recites that the offset phasor determiner operative to **store** the **previous channel impulse response** and **update** the **previous channel impulse response** with the phase corrected channel impulse response. In the cited sections, Nagayasu et al. does not describe using and updating previous channel impulse response as recited in claim 2 thus, there is no need for Nagayasu et al. to store previous channel impulse response. Further, as explained above, Nagayasu et al. uses two different values within the same frequency corrected burst as identified by units 12 and 14. Accordingly, claim 2 is further patentably distinguishable from Nagayasu et al.

Regarding claim 3, Applicants respectfully point to the Examiner that claim 3 recites that the offset vector is a product of 1) previous channel impulse response and 2) the **complex conjugate** of the current channel impulse response. In contrast, Nagayasu et al. describes that the phase deviation detecting means computes each product of the complex conjugate of channel impulse response estimated by units 12 and 14 (*see* col. 7, lines 14-18). Thus, Nagayasu et al. calculates the phase deviation completely differently than what is recited in clai 3. Accordingly, claim 3 is further patentably distinguishable from Nagayasu et al.

Regarding claim 4, the Examiner has stated that "Nagayasu discloses a system wherein the offset phasor **is computed by iteratively rotating a pair of vectors** (See column 8, lines 38-50). " Applicants respectfully point to the Examiner that in the cited sections, Nagayasu et al. describe functions of various elements without describing vector rotations as the Examiner has stated. Further, the Examiner has stated that "The direction of rotation is arbitrary and can be chosen to drive either y or z towards aero." (Emphasis added). Applicants respectfully disagree. The mathematics of vector rotation calculation is not arbitrary and a person skilled in the art will

not arbitrarily rotate vectors hoping to achieve the results as intended. The vector rotation is application specific based on the predetermined calculation. Nagayasu et al. does not describe arbitrarily rotating the vector to achieve the results and the Examiner has not cited reference in Nagayasu et al. that teach, suggest, or provide motivation for such rotation. Accordingly, claim 4 is further patentably distinguishable from Nagayasu et al.

Claim 8 is rejected in the manner of claim 1, accordingly claim 8 is patentably distinguishable from Nagayasu et al. for at least the same reasons as claim 1. Further, claim 8 has been amended to recite that the phase offset corrects the current channel impulse response by the phase offset using the offset phasor and provides a phase corrected channel impulse response wherein the offset phasor being at least partly a function of one or more of the average channel impulse response and a previous channel impulse response. As explained above, Nagayasu et al. does not teach this limitation. Accordingly, claim 8 is patentably distinguishable from Nagayasu et al.

Claims 9 and 10 have been canceled without prejudice or disclaimer of subject matter recited therein. Thus, the rejection of claims 9 and 10 has been rendered moot. Claim 11 depends from claim 8 and is patentably distinguishable from Nagayasu et al. for at least the same reasons as claim 8.

Claim 12 has been rejected in the manner of claim 1. Accordingly, claim 12 is patentably distinguishable from Nagayasu et al. for at least the same reasons as claim 1.

Claim 13 has been rejected in the manner of claim 2. Accordingly, claim 12 is patentably distinguishable from Nagayasu et al. for at least the same reasons as claim 2.

As to claim 14, the Examiner has stated that "Nagayasu discloses a system wherein the **sine and cosine** of the phase offset is iteratively computed using a first vector and a second vector (**See column 7, lines 13-24**)." Applicant respectfully points to the Examiner that in the cited sections, Nagayasu et al. does not describe what the Examiner has asserted. Accordingly, claim 14 is further patentably distinguishable form Nagayasu et al.

Claim 15 has been rejected in the manner of claim 1. Further, regarding claim 15, the Examiner has cited block 15 as a comparator and also as a vector analyzer as recited in claim 15. Applicants respectfully point to the Examiner that the reference must teach each and every limitation of claim 15. Nagayasu et al. does not describe each element as recited in claim 15. Further, the Examiner has used the offset vector representing a phase offset of the current channel impulse response as recited in claim 15 and stated that "the frequency corrector of Nagayasu has a linear relationship with a phase corrector of the current application.) **that computes** a corrected channel impulse response using the offset phasor." (Emphasis added). Applicant respectfully points to the Examiner that no where Nagayasu et al. describes using a phase offset representation for correcting frequency offset and the Examiner has also not cited any such teaching in the cited reference. Furthermore, claim 15 recites that the comparator computes an offset vector as a function of a current channel impulse response and a second channel impulse response. Nagayasu et al. does not teach this limitation. As explained above, Nagayasu et al. computes estimates at different positions within the same burst. Nagayasu et al do not describe determining an offset vector as a function of **a current channel** impulse response and **a second channel** impulse response. Accordingly, claim 15 is further patentably distinguishable from Nagayasu et al.

As to claim 16, the Examiner has cited block 16 of figure 1 in Nagayasu et al. Applicants respectfully request a careful reading of claim 16 and the description of block 16. Claim 16 recites that the **second channel impulse response** is one of an average channel impulse response and a previous channel impulse response where according to Nagayasu et al., block 16 is an averaging circuit configured to average the phase deviation detected by the phase deviation circuit 15 (*see* col. 8, lines 52-54). Further, block 15 actually computes the phase deviation based on two estimates calculated by blocks 12 and 14. Thus, the averaging block 16 averages the output of the combine result of both estimates. Therefore, Nagayasu et al. does not describe that the **second channel impulse response** is one of an average channel impulse response and a previous channel impulse response as recited in claim 16. Accordingly, claim 16 is further patentably distinguishable from Nagayasu et al.

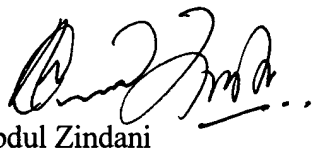
Claims 17-19 depend from claim 15 and are patentably distinguishable from Nagayasu et al. for at least the same reasons as claim 15 and explanation provided for distinguishing factors for other related claims.

Claims 20-21 have been canceled without prejudice and disclsimer of subject matter recited therein. Thus, the rejection of these claims has rendered moot.

Claim 26 has been amended to include the subject matter that the Examiner has identified to be allowable. Accordingly, claim 26 and those depend therefrom are patentably distinguishable from Nagayasu et al.

Applicant believes this application and the claims herein to be in a condition for allowance. Should the Examiner have further inquiry concerning these matters, please contact the below named attorney for Applicant.

Respectfully submitted,



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